	L #	Hits	Search Text	DBs
1	L2	36929	(fold$3 compound$3) near10 (instruction operation)	USPAT; US-PGPUB
2	L5	19226	(instruction prefetch$3 fetch$3) near10 (buffer queue)	USPAT; US-PGPUB
3	L7	9450	(fold$3 compound$3) near10 (instruction operation)	EPO; JPO; DERWENT; IBM_TDB
4	L8	6994	(instruction prefetch$3 fetch$3) near10 (buffer queue)	EPO; JPO; DERWENT; IBM_TDB
5	L6	83	2 near99 5	USPAT; US-PGPUB
6	L9	25	7 and 8	EPO; JPO; DERWENT; IBM_TDB
7	L10	9410	((fold$3 compound$3) near10 (instruction operation)).ab,ti.	EPO; JPO; DERWENT; IBM_TDB
8	L11	0	8 and 10 not 9	EPO; JPO; DERWENT; IBM_TDB
9	L12	21	8 and 10	EPO; JPO; DERWENT; IBM_TDB
10	L13	1445	((fold$3 compound$3) near10 (instruction operation)).ab,ti.	USPAT; US-PGPUB
11	L14	20	5 and 13 not 6	USPAT; US-PGPUB
12	L15	94521	(fold$3 compound$3 compress$3) near10 (instruction operation)	USPAT; US-PGPUB
13	L18	4867	((fold$3 compound$3 compress$3) near10 (instruction operation)).ab,ti.	USPAT; US-PGPUB
14	L20	35722	(fold$3 compound$3 compress$3) near10 (instruction operation)	EPO; JPO; DERWENT; IBM_TDB
15	L21	171	5 near99 15	USPAT; US-PGPUB
16	L24	31	8 and 20 not 9	EPO; JPO; DERWENT; IBM_TDB
17	L23	44	18 and 21	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	JP 2000081982 A	☐	COMPILER, PROCESSOR AND RECORDING MEDIUM	
2	JP 2000078522 A	☒	DYNAMIC PICTURE REPRODUCING DEVICE	
3	JP 10304310 A	☒	METHOD FOR RECORDING INFORMATION AND DEVICE THEREFOR	
4	JP 10116191 A	☒	PROCESSOR EQUIPPED WITH BUFFER FOR COMPRESSED INSTRUCTION	
5	JP 09261482 A	☒	DATA PROCESSOR	
6	JP 08328850 A	☒	CODE SIZE REDUCING MICROPROCESSOR	
7	JP 08263263 A	☒	DATA PROCESSOR AND COMPRESSED PROGRAM GENERATION DEVICE	
8	JP 08147139 A	☒	DATA PROCESSOR	
9	JP 07325805 A	☒	VECTOR PROCESSOR	
10	JP 06070286 A	☒	STILL PICTURE TRANSFER DEVICE	
11	JP 05324314 A	☒	DATA PROCESSOR	
12	JP 05054312 A	☒	ERROR RECOVERY SYSTEM FOR MAGNETIC TAPE	
13	JP 04359315 A	☒	DATA COMPRESSION CONTROLLER AND DATA RESTORATION CONTROLLER	
14	JP 04052923 A	☒	DATA INPUT/OUTPUT SYSTEM	
15	JP 02155037 A	☒	OPERATION METHOD FOR PIPELINED PROCESSING UNIT IN DIGITAL COMPUTER	
16	JP 61157946 A	☒	MICROCOMPUTER	
17	JP 61125641 A	☒	DATA COMPRESSION CONTROL SYSTEM	
18	JP 60239261 A	☒	CONTROLLING SYSTEM OF PRINTING OF CARD INFORMATION	
19	JP 60097778 A	☒	PICTURE DATA EXPANDER	
20	JP 59188779 A	☒	VECTOR PROCESSOR	
21	WO 38049 A1	☒	DEVICE AND METHOD FOR GENERATING AND EXECUTING COMPRESSED PROGRAMS OF A VERY LONG INSTRUCTION WORD PROCESSOR	
22	WO 9527244 A1	☒	COMPUTER SYSTEM	

	Document ID	U	Title	Current OR
23	US 20020 19908 3 A	☒	High code-density microcontroller architecture for low-end embedded system, selects decoding tables based on group prefix of compressed instruction to search original instruction	
24	WO 20028 9470 A	☒	Camera device has digital image data after the resolution degradation or buffered compressed data according to the instruction of a selection signal	
25	US 62438 36 B	☒	Circular buffering for on-chip real time debugging of program of embedded systems e.g. cellular phone, involves generating link component between adjacent trace codes of input stream to have circular buffer	
26	US 61991 26 B	☒	Data processing system has decompression engine which outputs fixed sized uncompressed program instruction to processor from variably sized compressed program instruction in memory	
27	JP 20000 35958 A	☒	Vector component instruction processor processes conversion command for compressing or expanding vector component, using data buffer whose storage area is smaller than number of vector components	
28	US 59305 08 A	☒	Wide instruction word storing and decoding method for microprocessor	
29	US 59013 18 A	☒	Code compiling method for computer system	
30	US 58193 08 A	☒	Instruction buffering and issuing method in superscalar microprocessor - involves obtaining linear systolic array containing several pointer entries, each entry having address and status portions for storing pointer and status associated with RAM entry	
31	JP 10116 191 A	☐	Instruction forwarding unit for cache memory for computer - controls writing operation in two buffers such that decompressed VLIW instruction precedes over compressed VLIW instruction stored in memory	

	Document ID	U	Title	Current OR
1	US 20030 22309 7 A1	☐	Image inputting apparatus, method, and storage medium recording image inputting program	358/471
2	US 20030 21287 9 A1	☒	Method and apparatus for object code compression and decompression for computer systems	712/208
3	US 20030 04651 9 A1	☒	Progressive instruction folding in a processor with fast instruction decode	712/226
4	US 20020 19908 3 A1	☒	High code-density microcontroller architecture with changeable instruction formats	712/209
5	US 20020 16994 6 A1	☒	Methods, systems, and computer program products for compressing a computer program based on a compression criterion and executing the compressed program	712/209
6	US 20020 16198 9 A1	☒	Apparatus and method for storing instruction set information	712/227
7	US 20020 05099 2 A1	☒	Geometry instructions for graphics data compression	345/423
8	US 20020 03541 2 A1	☒	Method and apparatus for controlling the strategy of compounding pharmaceutical admixtures	700/239
9	US 20010 01309 3 A1	☒	Instruction code conversion unit and information processing system and instruction code generation method	712/210
10	US 66913 05 B1	☒	Object code compression using different schemes for different instruction types	717/136
11	US 66813 19 B1	☒	Dual access instruction and compound memory access instruction with compatible address fields	712/208
12	US 66314 59 B1	☒	Extended instruction word folding apparatus	712/210
13	US 66256 71 B1	☒	Compression of buffered data	710/52
14	US 65643 14 B1	☒	Computer instruction compression	712/210
15	US 65321 21 B1	☒	Compression algorithm with embedded meta-data for partial record operation augmented with expansion joints	360/8
16	US 65320 12 B2	☒	Geometry instructions for graphics data compression	345/423
17	US 63016 51 B1	☒	Method and apparatus for folding a plurality of instructions	712/202
18	US 62759 21 B1	☒	Data processing device to compress and decompress VLIW instructions by selectively storing non-branch NOP instructions	712/24
19	US 62370 86 B1	☒	1 Method to prevent pipeline stalls in superscalar stack based computing systems	712/226
20	US 61991 26 B1	☒	Processor transparent on-the-fly instruction stream decompression	710/68

	Document ID	U	Title	Current OR
21	US 6185672 B1	☒	Method and apparatus for instruction queue compression	712/217
22	US 6108768 A	☒	Reissue logic for individually reissuing instructions trapped in a multiissue stack based computing system	712/214
23	US 6105112 A	☒	Dynamic folding of cache operations for multiple coherency-size systems	711/141
24	US 6044450 A	☒	Processor for VLIW instruction	712/24
25	US 6029240 A	☒	Method for processing instructions for parallel execution including storing instruction sequences along with compounding information in cache	712/23
26	US 6026485 A	☒	Instruction folding for a stack-based machine	712/226
27	US 5897219 A	☒	Recording/playback apparatus for digital video cassette recorder	386/111
28	US 5875325 A	☒	Processor having reduced branch history table size through global branch history compression and method of branch prediction utilizing compressed global branch history	712/240
29	US 5870576 A	☒	Method and apparatus for storing and expanding variable-length program instructions upon detection of a miss condition within an instruction cache containing pointers to compressed instructions for wide instruction word processor architectures	712/210
30	US 5819308 A	☒	Method for buffering and issuing instructions for use in high-performance superscalar microprocessors	711/108
31	US 5784585 A	☒	Computer system for executing instruction stream containing mixed compressed and uncompressed instructions by automatically detecting and expanding compressed instructions	712/209
32	US 5732234 A	☒	System for obtaining parallel execution of existing instructions in a particulr data processing configuration by compounding rules based on instruction categories	712/200
33	US 5652830 A	☒	Data storage device	358/1.16
34	US 5568650 A	☒	Control unit for controlling reading and writing of a magnetic tape unit	710/52
35	US 5504932 A	☒	System for executing scalar instructions in parallel based on control bits appended by compounding decoder	712/208
36	US 5502826 A	☒	System and method for obtaining parallel existing instructions in a particular data processing configuration by compounding instructions	712/213
37	US 5500942 A	☒	Method of indicating parallel execution compoundability of scalar instructions based on analysis of presumed instructions	712/210
38	US 5465377 A	☒	Compounding preprocessor for cache for identifying multiple instructions which may be executed in parallel	712/23
39	US 5459844 A	☒	Predecode instruction compounding	712/213
40	US 5448746 A	☒	System for comounding instructions in a byte stream prior to fetching and identifying the instructions for execution	712/210
41	US 5446850 A	☒	Cross-cache-line compounding algorithm for scism processors	712/215
42	US 5355460 A	☒	In-memory preprocessor for compounding a sequence of instructions for parallel computer system execution	712/215

	Document ID	U	Title	Current OR
43	US 5303356 A	☒	System for issuing instructions for parallel execution subsequent to branch into a group of member instructions with compoundability in dictation tag	712/238
44	US 5295249 A	☐	Compounding preprocessor for cache for identifying multiple instructions which may be executed in parallel	712/213

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2	L5	19226	(instruction prefetch$3 fetch$3) near10 (buffer queue)	USPAT; US-PGPUB
3	L7	9450	(fold$3 compound$3) near10 (instruction operation)	EPO; JPO; DERWENT; IBM_TDB
4	L8	6994	(instruction prefetch$3 fetch$3) near10 (buffer queue)	EPO; JPO; DERWENT; IBM_TDB
5	L6	83	2 near99 5	USPAT; US-PGPUB
6	L9	25	7 and 8	EPO; JPO; DERWENT; IBM_TDB
7	L10	9410	((fold$3 compound$3) near10 (instruction operation)).ab,ti.	EPO; JPO; DERWENT; IBM_TDB
8	L11	0	8 and 10 not 9	EPO; JPO; DERWENT; IBM_TDB
9	L12	21	8 and 10	EPO; JPO; DERWENT; IBM_TDB
10	L13	1445	((fold$3 compound$3) near10 (instruction operation)).ab,ti.	USPAT; US-PGPUB
11	L14	20	5 and 13 not 6	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20030228274 A1	☐	Polyamide chains of precise length	424/78.37
2	US 20030211990 A1	☒	Neural regeneration peptides and methods for their use in treatment of brain damage	514/12
3	US 20030181719 A1	☒	Novel heterocyclic antibacterial compounds	544/276
4	US 20030130172 A1	☒	Novel lipoglycopeptide antibiotics	514/8
5	US 20030109531 A1	☒	Therapeutic agent composition and method of use	514/249
6	US 20030087379 A1	☒	Assay for identifying inhibitors of HIV RT dimerization	435/69.1
7	US 20030046519 A1	☒	Progressive instruction folding in a processor with fast instruction decode	712/226
8	US 20030027755 A1	☒	Compositions and methods for the rescue of white matter	514/12
9	US 20020035412 A1	☒	Method and apparatus for controlling the strategy of compounding pharmaceutical admixtures	700/239
10	US 20010031497 A1	☒	Chitosan related compositions and methods for delivery of nucleic acids and oligonucleotides into a cell	435/455
11	US 6693079 B1	☒	Insulin-like growth factor agonist molecules	514/14
12	US 6693078 B1	☒	Insulin-like growth factor agonist molecules	514/14
13	US 6689751 B1	☒	Insulin-like growth factor agonist molecules	514/14
14	US 6683053 B1	☒	Insulin-like growth factor agonist molecules	514/13
15	US 6681319 B1	☒	Dual access instruction and compound memory access instruction with compatible address fields	712/208
16	US 6680298 B1	☒	Insulin-like growth factor agonist molecules	514/14
17	US 6677305 B1	☒	Insulin-like growth factor agonist molecules	514/12
18	US 6645775 B1	☒	Insulin-like growth factor agonist molecules	436/518
19	US 6635619 B1	☒	Insulin-like growth factor agonist molecules	514/14

	Document ID	U	Title	Current OR
20	US 6632794 B1	☒	Insulin-like growth factor agonist molecules	514/13
21	US 6631459 B1	☒	Extended instruction word folding apparatus	712/210
22	US 6620789 B1	☒	Insulin-like growth factor agonist molecules	514/14
23	US 6608031 B1	☒	Insulin-like growth factor agonist molecules	514/15
24	US 6552167 B1	☒	Polyamide chains of precise length	530/326
25	US 6548645 B1	☒	Immunoassay for 2-oxo-3-hydroxy LSD	530/405
26	US 6532521 B1	☒	Mechanism for high performance transfer of speculative request data between levels of cache hierarchy	711/137
27	US 6510494 B1	☒	Time based mechanism for cached speculative data deallocation	711/137
28	US 6496921 B1	☒	Layered speculative request unit with instruction optimized and storage hierarchy optimized partitions	712/207
29	US 6487637 B1	☒	Method and system for clearing dependent speculations from a request queue	711/133
30	US 6473833 B1	☒	Integrated cache and directory structure for multi-level caches	711/122
31	US 6438656 B1	☒	Method and system for cancelling speculative cache prefetch requests	711/137
32	US 6421763 B1	☒	Method for instruction extensions for a tightly coupled speculative request unit	711/137
33	US 6421762 B1	☒	Cache allocation policy based on speculative request history	711/130
34	US 6418516 B1	☒	Method and system for managing speculative requests in a multi-level memory hierarchy	711/138
35	US 6393528 B1	☒	Optimized cache allocation algorithm for multiple speculative requests	711/137
36	US 6360299 B1	☒	Extended cache state with prefetched stream ID information	711/137
37	US 6321303 B1	☒	Dynamically modifying queued transactions in a cache memory system	711/140
38	US 6311254 B1	☒	Multiple store miss handling in a cache memory memory system	711/126
39	US 6301651 B1	☒	Method and apparatus for folding a plurality of instructions	712/202
40	US 6275903 B1	☒	Stack cache miss handling	711/132
41	US 6269427 B1	☒	Multiple load miss handling in a cache memory system	711/140
42	US 6251865 B1	☒	Insulin-like growth factor agonist molecules	514/15

	Document ID	U	Title	Current OR
43	US 6237086 B1	☒	1 Method to prevent pipeline stalls in superscalar stack based computing systems	712/226
44	US 6237085 B1	☒	Processor and method for generating less than (LT), Greater than (GT), and equal to (EQ) condition code bits concurrent with a logical or complex operation	712/223
45	US 6232076 B1	☒	Stabilizer of dye sequencing products	435/6
46	US 6184037 B1	☒	Chitosan related compositions and methods for delivery of nucleic acids and oligonucleotides into a cell	435/455
47	US 6184027 B1	☒	Isolation and purification of eubacteria and fungus with catalytically inactive murein binding enzymes	435/261
48	US 6182201 B1	☒	Demand-based issuance of cache operations to a system bus	711/202
49	US 6173371 B1	☒	Demand-based issuance of cache operations to a processor bus	711/146
50	US 6171578 B1	☒	Benzodiazepine derivatives for imaging thrombi	424/1.69
51	US 6170050 B1	☒	Length decoder for variable length data	712/210
52	US 6159719 A	☒	Pan-bacterial and pan-fungal identification reagents and methods of use thereof	435/206
53	US 6122638 A	☒	Object-oriented processor and method for caching intermediate data in an object-oriented processor	707/103Y
54	US 6121416 A	☒	Insulin-like growth factor agonist molecules	530/326
55	US 6108768 A	☒	Reissue logic for individually reissuing instructions trapped in a multiissue stack based computing system	712/214
56	US 6105112 A	☒	Dynamic folding of cache operations for multiple coherency-size systems	711/141
57	US 6090573 A	☒	Detecting eubacteria and fungus and determining their antibiotic sensitivity by using catalytically inactive murein binding enzymes	435/32
58	US 6035390 A	☒	Method and apparatus for generating and logically combining less than (LT), greater than (GT), and equal to (EQ) condition code bits concurrently with the execution of an arithmetic or logical operation	712/220
59	US 6029240 A	☒	Method for processing instructions for parallel execution including storing instruction sequences along with compounding information in cache	712/23
60	US 6026485 A	☒	Instruction folding for a stack-based machine	712/226
61	US 5962281 A	☒	Process for preparing L-tertiary-leucine and L-phosphinothricine by transamination	435/116
62	US 5935804 A	☒	Method for detecting eubacteria in biological samples with catalytically inactive murein binding enzymes	435/18
63	US 5919669 A	☒	Process for preparing L-tertiary-leucine and L-phosphinothricine by transamination	435/106
64	US 5901307 A	☒	Processor having a selectively configurable branch prediction unit that can access a branch prediction utilizing bits derived from a plurality of sources	712/240

	Document ID	U	Title	Current OR
65	US 58753 25 A	☒	Processor having reduced branch history table size through global branch history compression and method of branch prediction utilizing compressed global branch history	712/240
66	US 57649 40 A	☒	Processor and method for executing a branch instruction and an associated target instruction utilizing a single instruction fetch	712/206
67	US 57534 70 A	☒	Process for preparing L-tertiary-Leucine and L-phosphinothricine by transamination	435/116
68	US 57520 14 A	☒	Automatic selection of branch prediction methodology for subsequent branch instruction based on outcome of previous branch prediction	712/240
69	US 57404 19 A	☒	Processor and method for speculatively executing an instruction loop	712/241
70	US 57322 34 A	☒	System for obtaining parallel execution of existing instructions in a particulr data processing configuration by compounding rules based on instruction categories	712/200
71	US 57014 30 A	☒	Cross-cache-line compounding algorithm for scism processors	711/118
72	US 55049 32 A	☒	System for executing scalar instructions in parallel based on control bits appended by compounding decoder	712/208
73	US 55028 26 A	☒	System and method for obtaining parallel existing instructions in a particular data processing configuration by compounding instructions	712/213
74	US 55009 42 A	☒	Method of indicating parallel execution compoundability of scalar instructions based on analysis of presumed instructions	712/210
75	US 54653 77 A	☒	Compounding preprocessor for cache for identifying multiple instructions which may be executed in parallel	712/23
76	US 54598 44 A	☒	Predecode instruction compounding	712/213
77	US 54487 46 A	☒	System for comounding instructions in a byte stream prior to fetching and identifying the instructions for execution	712/210
78	US 54468 50 A	☒	Cross-cache-line compounding algorithm for scism processors	712/215
79	US 53554 60 A	☒	In-memory preprocessor for compounding a sequence of instructions for parallel computer system execution	712/215
80	US 53033 56 A	☒	System for issuing instructions for parallel execution subsequent to branch into a group of member instructions with compoundability in dictation tag	712/238
81	US 52952 49 A	☒	Compounding preprocessor for cache for identifying multiple instructions which may be executed in parallel	712/213
82	US 52874 67 A	☒	Pipeline for removing and concurrently executing two or more branch instructions in synchronization with other instructions executing in the execution unit	712/235
83	US 52652 13 A	☐	Pipeline system for executing predicted branch target instruction in a cycle concurrently with the execution of branch instruction	712/240

	Document ID	U	Title	Current OR
1	JP 20030 91414 A	☐	PROGRESSIVE INSTRUCTION FOLDING IN PROCESSOR WITH FAST INSTRUCTION DECODE	
2	JP 08202 616 A	☒	CENTRAL ARITHMETIC PROCESSING UNIT AND INFORMATION PROCESSING SYSTEM	
3	JP 06067 710 A	☒	PROGRAMMABLE CONTROLLER	
4	JP 05165 659 A	☒	MICROPROCESSOR	
5	JP 61016 350 A	☒	BUFFER STORAGE DEVICE OF INFORMATION PROCESSOR	
6	EP 12781 19 A2	☒	Progressive instruction folding in a processor with fast instruction decoding	
7	EP 99291 6 A1	☒	Digital signal processor	
8	EP 99289 2 A1	☒	Compound memory access instructions	
9	DE 32358 14 A1	☒	Circuit arrangement for recoding a binary digital information flow into an nB/(n+1) B line code	
10	NN950 6163	☒	Half-Cycle Branch Folding within an Instruction Buffer	
11	NN930 8565	☒	Decode Compound Checker	
12	NN920 1330	☒	Using History to Improve the Handling of Address Generation Interlocks in Branch Instructions.	
13	NB910 3336	☒	Compounding Instructions in the Execution Unit.	
14	NN710 7660	☒	System for Interlocking between Asynchronously Operating Indexing Arithmetic Units. July 1971.	
15	NN710 7656	☒	System for Interlocking Between Asynchronously Operating Indexing and Arithmetic Units. July 1971.	
16	KR 20030 67364 A	☒	Device and method for folding instruction of eisc processor	
17	WO 20030 86323 A	☒	Treatment of immune system disorder e.g. autoimmune disorder and inflammatory disorder involves increasing the concentration of a Gly-Pro-Glu related compound in the central nervous system	
18	WO 20030 56340 A	☒	Use of Fas associated protein with dead domain, and cellular phosphorylated p38-mitogen activated protein kinases as a biological indicator of tumor status	
19	US 20030 02775 5 A	☒	Restoration of myelination of axons due to neuronal injury or disease e.g. multiple sclerosis involves use of insulin-like growth factor	
20	EP 12781 19 A	☒	Progressive instruction folding in a processor with fast instruction decoding, where a fold decoder determines whether the successive entries in the instruction fetch buffer contain instructions which may be folded	
21	WO 20030 12127 A	☒	Measuring hetero/homodimerization of HIV reverse transcriptase, by contacting p66 subunit in presence of dissociation agent with p51/p66 subunit, incubating with reassociation buffer to form a complex, detecting complex	
22	WO 20022 5252 A	☒	Detecting the presence and amount of fluoride in test sample, e.g. water system, involves contacting the test sample with chromophore- or fluorophore-containing compound	

	Document ID	U	Title	Current OR
23	KR 20010 63191 A	☒	Eisc processor	
24	US 61051 12 A	☒	Cache instruction managing method for use in computer system, involves comparing entries of queue with new cache instructions to determine instruction redundancy	
25	EP 99289 2 A	☐	Processor has an instruction buffer and decoder operable to decode both single and compound instructions stored in the buffer dependent on a tag in the buffer	

	Document ID	U	Title	Current OR
1	US 20020 14787 2 A1	☐	Sequentially performed compound compare-and-swap	710/200
2	US 66585 78 B1	☒	Microprocessors	713/324
3	US 66257 22 B1	☒	Processor controller for accelerating instruction issuing rate	712/16
4	US 64776 39 B1	☒	Branch instruction mechanism for processor	712/237
5	US 64185 14 B1	☒	Removal of posted operations from cache operations queue	711/133
6	US 63569 97 B1	☒	Emulating branch instruction of different instruction set in a mixed instruction stream in a dual mode system	712/237
7	US 63473 61 B1	☒	Cache coherency protocols with posted operations	711/141
8	US 63453 40 B1	☒	Cache coherency protocol with ambiguous state for posted operations	711/141
9	US 63306 43 B1	☒	Cache coherency protocols with global and local posted operations	711/141
10	US 61923 84 B1	☒	System and method for performing compound vector operations	708/200
11	US 61450 59 A	☒	Cache coherency protocols with posted operations and tagged coherency states	711/143
12	US 57218 54 A	☒	Method and apparatus for dynamic conversion of computer instructions	712/203
13	US 55985 46 A	☒	Dual-architecture super-scalar pipeline	712/209
14	US 55926 34 A	☒	Zero-cycle multi-state branch cache prediction data processing system and method thereof	712/239
15	US 55420 59 A	☒	Dual instruction set processor having a pipeline with a pipestage functional unit that is relocatable in time and sequence order	712/41
16	US 54758 53 A	☒	Cache store of instruction pairs with tags to indicate parallel execution	712/213
17	US 53983 21 A	☒	Microcode generation for a scalable compound instruction set machine	712/216
18	US 52147 63 A	☒	Digital computer system capable of processing two or more instructions in parallel and having a coche and instruction compounding mechanism	712/212
19	US 51971 35 A	☒	Memory management for scalable compound instruction set machines with in-memory compounding	712/217
20	US 42192 96 A	☐	Automatic storage and retrieval apparatus for individual file folders	414/273

	L #	Hits	Search Text	DBs
1	L2	36929	(fold$3 compound$3) near10 (instruction operation)	USPAT; US-PGPUB
2	L5	19226	(instruction prefetch$3 fetch$3) near10 (buffer queue)	USPAT; US-PGPUB
3	L7	9450	(fold$3 compound$3) near10 (instruction operation)	EPO; JPO; DERWENT; IBM_TDB
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